

**AMENDMENTS TO THE DRAWINGS**

The attached sheets of drawings include changes to Figures 12-14. These sheets, which include Figures 12-14, replace the original sheets including Figures 12-14.

Attachment: Replacement Sheets (2)

### **REMARKS**

Claims 1-11 are pending in the current application. Of those, claims 1 and 11 are independent claims. Claims 1-3 are amended by this Response. New claims 10 and 11 are added by this Response. No claims are canceled by this Response.

### **Specification**

The Examiner asserts the title is not descriptive. Applicant respectfully submits that the title is amended to be more clearly indicative of the example embodiments to which the claims are directed.

### **Drawings**

The Examiner asserts FIGS. 12-14 should be designated by a legend such as “prior art” because only that which is old is illustrated. Applicant respectfully submits that replacement sheets including FIGS. 12-14 designated by the legend “Conventional Art” are submitted concurrently with the present Response.

### **Discussion of Example Embodiments**

Example embodiments may include a rewritable and nonvolatile display memory 7 and adjustment data for gamma correction may be stored in the display memory 7 separately from display data D. For example, as shown at FIG. 1, adjustment data for the gamma correction may be provided via terminals (H1, H2, and H3) that are different from terminals (R1in to R6in, B1in to B6in, and G1in to G6in) to be provided with the display data D (see the last paragraph at page 14 to the second paragraph at page 30 of Applicant’s specification). This provision of the rewritable and nonvolatile display memory 7 may make it possible to rewrite the adjustment data

in the display memory 7. Because the adjustment data in the display memory 7 may not be deleted but kept stored, it may be possible to repeatedly read and use the same adjustment data. For example, in an example embodiment, only correction characteristics that are a part of the adjustment data may be easily changed.

### **Claims Rejections**

Claims 1-4 and 8 are stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nakao (US 2001/0003431, hereinafter Nakao). Claims 6, 7 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakao in view of Applicant's Alleged Admitted Prior Art (hereinafter AAPA). Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakao in view of Nakamura (US 2003/0043132, hereinafter Nakamura). Applicant respectfully traverses these rejections.

Nakao discloses at paragraph [0106] "by adding the adjustment data to the display data, display of a higher quality can be obtained by adjusting the reference voltage for gray scale display every horizontal line of the LCD panel and correcting the horizontal shadowing, or one display defect of the LCD panel." Therefore, Nakao discloses the adjustment data for a gamma correction is added to the display data and supplied.

Further, Applicant respectfully submits that the Examiner at page 2 of the current Office Action appears to find that the data latch circuit 43 as described at paragraph [0091] of Nakao corresponds to the "memory" of Applicant's claim 1. However, Nakao at paragraph [0094] discloses that the display data to which the adjustment data for the gamma correction is added is written into the data latch circuit 43. Therefore, the adjustment data for the gamma correction and the display data are not separately written into the data latch circuit 43. Moreover, Applicant respectfully submits that the latch circuit only temporarily holds data for each bit and is volatile.

Data written into the latch circuit is lost if the power supply to the latch circuit stops. Even assuming for the sake of argument an arrangement such that last data during the power supply remains in the latch circuit, data earlier than the last data is not stored. As such, an amount of data that the latch circuit can hold is very small and the data in the latch circuit is temporary. Therefore, one skilled in the art would recognize that the latch circuit is completely different from the “memory” of Applicant’s claim 1.

Further, because the data latched in the data latch circuit 43 is merely temporarily held, the same data cannot be repeatedly read and used. Therefore, it is not possible to change only correction characteristics that are a part of the adjustment data, and in a case where an attempt to change the adjustment data is made, the original data cannot be kept.

Accordingly, Applicant respectfully submits that Nakao fails to disclose “a memory section for separately storing  $\gamma$ -correction adjustment data and display data, the memory section being rewritable and nonvolatile; and a control section for controlling the  $\gamma$ -correction adjustment section so as to change the reference voltages on which the  $\gamma$ -correction has been performed in accordance with the  $\gamma$ -correction adjustment data, supplied from the memory section via terminals different from terminals via which the display data is supplied, the control section decreasing display unevenness between pixels that are adjacent to one another in at least one of the first and the second directions” as required by claim 1.

Applicant further addresses the Examiner’s improper combination of Nakao and AAPA. Applicant respectfully submits that one skilled in the art would not have a reason to combine AAPA with Nakao. In particular, the Examiner provides no reason for combining AAPA with Nakao, even if AAPA were admitted prior art (which Applicant does not admit). Nakao has nothing to do with reducing visibility of joint lines between a plurality of separate panels bonded together, and thus would provide no reason for combining its teaching to that of AAPA.

Accordingly, Applicant respectfully submits that claim 1 is patentable for at least the above reasons. Further, Applicant respectfully submits that even assuming for the sake of argument Nakao, Nakamura and/or AAPA are properly combinable (which Applicant does not admit), Nakamura and/or AAPA fail to cure the deficiencies of Nakao discussed above in regards to claim 1. Applicant also submits that claims 2-9, which depend from claim 1, are patentable for at least the same reasons discussed above in regards to claim 1 as well as on their own merits.

In view of the above, Applicant respectfully requests the rejections under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) be withdrawn.

#### **New Claims**

Applicant respectfully submits that new claim 10, which depends from claim 1, is patentable for at least the same reasons discussed above in regards to claim 1 as well as on its own merits.

Further, Applicant respectfully submits that new claim 11 is written so as to invoke the language of 35 U.S.C. § 112, sixth paragraph. Applicant also submits that new claim 11 contains features somewhat similar to those discussed above in regards to claim 1, and therefore, claim 11 is patentable for at least somewhat similar reasons as claim 1.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of the claims in connection with the present application is earnestly solicited.

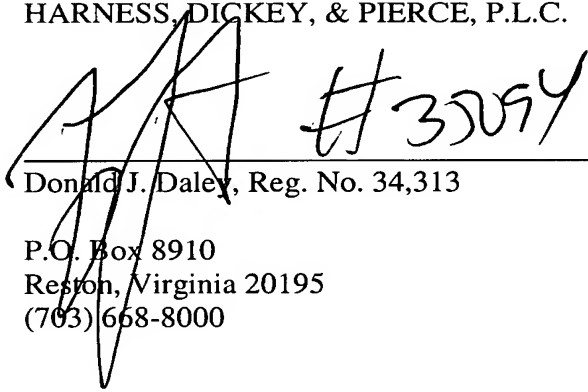
Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNES, DICKEY, & PIERCE, P.L.C.

By

 #35054  
\_\_\_\_\_  
Donald J. Daley, Reg. No. 34,313

P.O. Box 8910  
Reston, Virginia 20195  
(703) 668-8000

DJD/AAM: tlt